REMARKS

Claims 21-40, all the claims presently pending in this application, stand rejected on prior art grounds. Claims 35-40 stand rejected upon informalities. Claims 21, 29, and 35-37 are amended herein. The Applicant respectfully traverses the rejections based on the following discussion.

I. The Claim Rejections

A. The 35 U.S.C. §112, Second Paragraph, Rejections

Claims 35-40 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. These rejections are traversed as explained below.

The Applicant has amended claim 35 to remove the language pertaining to the ground voltage, wherein it is clear that the comparator cycles between an analog and digital configuration based on a selective selection of the input signal going through the transmission gates. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections to the claims.

B. The Prior Art Rejections

Claims 21-40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ono (U.S. Publication No. 2001/0007443A1), in view of Ishii (U.S. Patent No. 6,886,066). Applicants respectfully traverse these rejections based on the following discussion.

Ono teaches an OTA circuit disposed between a differential pair composed of NMOS

transistors and an NMOS follower transistor that composes an output buffer circuit. The OTA circuit generates a compensation current that is equal to a current that flows in a capacitance formed between the gate and the drain of each of the differential pair transistors and that flows in the reverse direction thereof. The compensation current cancels the current that flows in the capacitance formed between the gate and the drain of each of the differential pair transistors. Thus, a differential amplifier that has a high accuracy and, high gain, and a wide frequency band and that operates at a low power voltage can be accomplished. Using a differential amplifier having a high gain and a wide frequency band, a comparator that operates at high speed and an A/D converter using such a comparator can be accomplished.

Ishii teaches a method and apparatus for sharing signal pins on an interface between a system controller and peripheral integrated circuits reduces the number of signal pins required on a system controller integrated circuit. Signals of differing types are qualified by an internal peripheral select signal from which chip select signals for a plurality of externally interfaced peripheral integrated circuits are generated. The interface functions so that a single signal pin may be used for carrying different signal types between the system controller and each of the peripheral integrated circuits. The use of the internal peripheral select signal ensures that the setup times for the selection circuitry and pin drivers are met before a chip select signal enables communication with a selected peripheral and that a hold time is maintained for signals on shared interface pins so that the peripheral integrated circuits receive valid inputs from shared pins.

The claimed invention, as provided in amended independent claims 21, 29, and 35 include features, which are patentably distinguishable from the prior art references of record.

With respect to claims 21-23, and 29-32, contrary to the assertion in the Office Action, Figure 11 in Ono does not show a comparator cycling between an analog configuration and a digital configuration. The comparator in Ono operates in an "auto zero" mode and an "amp" mode, which are both "analog" modes since input transistors 1 and 2 are always operating in the saturation region (see also pages 7-8 of Ono, paragraphs [0095] through [0098]), which is not the case in the Applicant's invention. In Figure 5 of Ono, the tail current source 3 is always ON and enabled, whether the comparator is in the "auto zero" mode or the "amp" mode. Conversely, this is not the case in the Applicant's invention since the tail current source is only enabled in the analog configuration.

With respect to claims 24, 25-27, 33, and 34, those skilled in the art would readily acknowledge that it is absolutely untrue that "every comparator performs with hysteresis (or Schmitt trigger)" as concluded on page 3 of the Office Action. Also the statement on page 3 of the Office Action, "[w]hen the W/L ratios of the transistors are not equal, the asymmetric Schmitt triggering happens" is also absolutely untrue. Furthermore, adjusting the W/L ratio of the transistors of the comparator in Figure 5 of Ono will not cause the circuit to have the characteristics of an asymmetric Schmitt trigger. A Schmitt trigger characteristic is achieved through circuit topology as well as correct device sizes. Moreover, there is no Schmitt trigger topology or no circuit topology that provides characteristics of a Schmitt trigger in Figure 5 or Figure 11 of Ono.

With respect to claims 36-37, in Figure 11 of Ono, transistors 7 and 8 represent load transistors and are configured as MOSFET active load resistors. The "second pair of transistors" (T4 & T5) in Figure 1 of the Applicant's invention are configured as a current mirror, not active

resistor loads. Also in the Applicant's invention, the invertors at the output node of the comparator are used to buffer the output signal. The buffered version is then tapped off at two locations (n1 & n2) and fed back as two signals to control the transmission gates. This feature is not taught, suggested, or rendered obvious in Ono or Ishii.

There is no teaching in either Ono or Ishii that a majority of a cycle time of the comparator is spent in a digital configuration. The Office Action argues inherency in this regard (see page 4 of the Office Action as it pertains to claim 35), wherein it states, "[i]f the level of the reference voltage is set to be low, the majority of the cycle time will be [in] the digital configuration." However, there is no teaching in Ono that such a situation exists. Rather, the Office Action tends to suggest that Ono works in this manner although Ono itself renders no such teaching or suggestion.

Insofar as references may be combined to teach a particular invention, and the proposed combination of Ono and Ishii with one another, case law establishes that, before any prior-art references may be validly combined for use in a prior-art 35 U.S.C. § 103(a) rejection, the individual references themselves or corresponding prior art must suggest that they be combined.

For example, in In re Semaker, 217 U.S.P.Q. 1, 6 (C.A.F.C. 1983), the court stated: "[P]rior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings." Furthermore, the court in Uniroyal, Inc. v. Rudkin-Wiley Corp., 5 U.S.P.Q.2d 1434 (C.A.F.C. 1988), stated, "[w]here prior-art references require selective combination by the court to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. . . . Something in the prior art must suggest the

desirability and thus the obviousness of making the combination."

In the present application, the reason given to support the proposed combination is improper, and is not sufficient to selectively and gratuitously substitute parts of one reference for a part of another reference in order to try to meet, but failing nonetheless, the Applicant's novel claimed invention. Furthermore, the claimed invention meets the above-cited tests for obviousness by including the embodiments such as, "...wherein said plurality of invertors are operable to buffer said output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates." As such, all of the claims of this application are, therefore, clearly in condition for allowance, and it is respectfully requested that the Examiner pass these claims to allowance and issue.

As declared by the Federal Circuit:

> In proceedings before the U.S. Patent and Trademark Office, the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art. The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. In re Fritch, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992) citing In re Fine, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988).

Here, the Examiner has not met the burden of establishing a prima facie case of obviousness. It is clear that, not only does Ono fail to disclose all of the elements of the claims of the present invention, particularly "wherein said plurality of invertors are operable to buffer said output signal, wherein the buffered output signal is returned as two signals to control said plurality of transmission gates" but also, if combined with Ishii, fails to disclose these elements as well. The unique elements of the claimed invention are clearly an advance over the prior art.

The Federal Circuit also went on to state:

> The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. . . . Here the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. This court has previously stated that one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. Fritch at 1784-85, citing In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984).

Here, there is no suggestion that Ono, alone or in combination Ishii teaches a structure and method containing all of the limitations of the claimed invention. Consequently, there is absent the "suggestion" or "objective teaching" that would have to be made before there could be established the legally requisite "prima facie case of obviousness." Furthermore, Ono and Ishii are in two separate and wholly unique areas of technology. In fact, the USPTO has affirmed this by classifying Ono in U.S. Class 341, Subclass 159, and classifying Ishii in U.S. Class 710, Subclass 305.

In view of the foregoing, the Applicant respectfully submits that the collective cited prior art references do not teach or suggest the features defined by amended independent claims 21, 29, and 35 and as such, claims 21, 29, and 35 are patentable over Ono alone or in combination with Ishii. Further, dependent claims 22-28, 30-34, and 36-40 are similarly patentable over Ono alone or in combination with Ishii, not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define. Thus, the Applicant respectfully requests that these rejections be reconsidered and withdrawn.

Moreover, the Applicant notes that all claims are properly supported in the specification and accompanying drawings. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, the Applicant hereby submits that claims 21-40, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney=s Deposit Account Number 09-0456.

Respectfully submitted,

Dated: September 15, 2005

Mohammad S. Rahman
Registration No. 43,029
McGinn & Gibb, P.L.L.C.
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (301) 261-8625
Fax: (301) 261-8825
Customer Number: 29154